# University of Mumbai <br> Examination 2020 under cluster 9 (FAMT) <br> These are sample MCQs to indicate pattern, may or may not appeared in examination 

Program: BE Electronics and Telecommunication Engineering
Curriculum Scheme: R_2012
Examination: Third Year Semester V
Course Code: ETC 501 and Course Name: Microcontroller and Applications
Time: 1 hour
Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

| Q1. | The SP is of __ wide register. And this may be defined anywhere in the |
| :--- | :--- |
| Option A: | 8 byte, on-chip 128 byte RAM. |
| Option B: | 8 bit, on chip 256 byte RAM. |
| Option C: | 16 bit, on-chip 128 byte ROM |
| Option D: | 8 bit, on chip 128 byte RAM. |
|  |  |
| Q2. | After reset, SP register is initialized to address _ |
| Option A: | 08h |
| Option B: | 09 h |
| Option C: | 07h |
| Option D: | OFh |
|  |  |
| Q3. | What is the address range of SFR Register bank in 8051? |
| Option A: | $00 \mathrm{H}-77 \mathrm{H}$ |
| Option B: | $40 \mathrm{H}-80 \mathrm{H}$ |
| Option C: | $80 \mathrm{H}-7 \mathrm{FH}$ |
| Option D: | $80 \mathrm{H}-\mathrm{FFH}$ |
|  |  |
| Q4. | The 8051 microcontroller has |
| Option A: | 8 |
| Option B: | 16 |
| Option C: | 32 |
| Option D: | 64 |
|  |  |
| Q5. | In 8051 which interrupt has highest priority? bit-addressable memory. |
| Option A: | IE1 |
| Option B: | TF0 |
| Option C: | IEO |
| Option D: | TF1 |
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| Q6. | 8051 microcontroller has ___ internal RAM \& ___ internal ROM: |
| :---: | :---: |
| Option A: | 128 Byte, 4KB |
| Option B: | 128 Byte, 8KB |
| Option C: | 64 Byte, 4 KB |
| Option D: | 64 Byte, 8 KB |
|  |  |
| Q7. | The 8051 can handle ___ interrupt sources. (Excluding RESET) |
| Option A: | 3 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 6 |
|  |  |
| Q8. | Which bit/s play/s a significant role in the selection of a bank register of Program Status Word (PSW)? |
| Option A: | CY AND AC |
| Option B: | FO and OV |
| Option C: | RS0 and RS1 |
| Option D: | OV and $P$ |
|  |  |
| Q9. | Which bit must be set in TCON register in order to start the 'Timer 0' while operating in 'Mode 0'? |
| Option A: | TR0 |
| Option B: | TF0 |
| Option C: | IT0 |
| Option D: | IE0 |
|  |  |
| Q10. | In 8 bit signed number operations, OV flag is set to 1 if: |
| Option A: | a carry is generated from D7 bit |
| Option B: | a carry is generated from D3 bit |
| Option C: | a carry is generated from D7 or D3 bit |
| Option D: | a carry is generated from D7 or D6 bit |
|  |  |
| Q11. | When an interrupt is enabled, then where does the pointer (PC) moves immediately after this interrupt has occurred? |
| Option A: | to the next instruction which is to be executed |
| Option B: | to the last instruction of ISR |
| Option C: | to the first location of the memory called the interrupt vector table |
| Option D: | to the end of the program |
|  |  |
| Q12. | 8 input DAC has |
| Option A: | 8 discrete voltage levels |
| Option B: | 64 discrete voltage levels |
| Option C: | 124 discrete voltage levels |
| Option D: | 256 discrete voltage levels |
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| Q13. | What is the principle on which electromagnetic relays operate? |
| :---: | :---: |
| Option A: | electromagnetic induction |
| Option B: | motor control |
| Option C: | switching |
| Option D: | On-off-On |
|  |  |
| Q14. | How many registers are there in ARM7? |
| Option A: | 35 register( 28 GPR and 7 SPR) |
| Option B: | 37 registers(28 GPR and 9 SPR) |
| Option C: | 37 registers(31 GPR and 6 SPR) |
| Option D: | 35 register(30 GPR and 5 SPR) |
|  |  |
| Q15. | How many registers are accessible for ARM7 instruction set? |
| Option A: | All 15 general purpose |
| Option B: | 8 General purpose registers plus PC |
| Option C: | 8 General purpose registers |
| Option D: | All 15 general purpose plus PC |
|  |  |
| Q16. | $\qquad$ instruction puts the processor into supervisor mode and begins executing instructions from address $0 \times 08$. |
| Option A: | STMFD |
| Option B: | LDMFD |
| Option C: | LDREQB |
| Option D: | SWI |
|  |  |
| Q17. | Which among the following data processing instructions does not use the barrel shifter? |
| Option A: | ADD R2, R5, R4 |
| Option B: | MOV R5, R4, LSL \#2 |
| Option C: | MOV r5, R4, LSR \#2 |
| Option D: | MOV r5, R4, ROR \#2 |
|  |  |
| Q18. | Status of $Z$ flag after the execution of CMP instruction given below, when $\mathrm{RO}=12 ; \mathrm{R9}=12 \text {; is }$ <br> CMP RO, R9 |
| Option A: | $\mathrm{Z}=1$ |
| Option B: | $\mathrm{Z}=0$ |
| Option C: | Same as previous value |
| Option D: | Z= Infinite |
|  |  |
| Q19. | The BEQ instructions is used ___ |
| Option A: | To check the equality condition between the operands and then branch |
| Option B: | To check if the Operand is greater than the condition value and then branch |
| Option C: | To check if the flag Z is set to 1 and then causes branch |
| Option D: | To set THUMB mode if operands are equal |

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| :--- | :--- |
| Q20. | Identify wrong sentence |
| Option A: | Microprocessor is an IC which has only the CPU |
| Option B: | Microprocessors don't have RAM, ROM, |
| Option C: | Microprocessors don't have other peripheral on the chip. |
| Option D: | Microprocessor are based on Harward achitecture. |
|  |  |
| Q21. | This is not a Examples of embedded systems |
| Option A: | Laptop |
| Option B: | Digital Camera |
| Option C: | Smart TV |
| Option D: | Washing Machine |
|  |  |
| Q22. | What is the maximum capability of addressing the off-chip data memory \& off- <br> chip program memory in 8051? |
| Option A: | 8 K |
| Option B: | 16 K |
| Option C: | 32 K |
| Option D: | 64 K |
|  |  |
| Q23. | After reset of 8051, all ports are written with |
| Option A: | 00 H |
| Option B: | FFh |
| Option C: | 77 h |
| Option D: | AAh |
|  |  |
| Q24. | The 8051 can handle |
| Option A: | 3 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 6 |
|  |  |
| Q25. | 8051 has |
| Option A: | 3 |
| Option B: | 2 |
| Option C: | 1 |
| Option D: | 0 |

