

University of Mumbai
Examination 2020 under cluster 9 (FAMT)

These are sample MCQs to indicate pattern, may or may not appeared in examination

Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: ECC501 and Course Name: Microprocessor & Peripheral Interfacing

Time: 1 hour

Max. Marks: 50

=====

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The 8086 microprocessor is a_____ processor
Option A:	8 bit
Option B:	16 bit
Option C:	32 bit
Option D:	4 bit
Q2.	The BIU prefetch the instruction from memory and store them in_____
Option A:	Instruction Queue
Option B:	Instruction Pointer
Option C:	Stack Pointer
Option D:	Memory
Q3.	Select the control word of 8255 to initialize port A as input port, port B & C as output port, group A in mode 0 and group B in mode1
Option A:	Control word=90 H
Option B:	Control word=91 H
Option C:	Control word=94 H
Option D:	Control word=92 H
Q4.	The number of inputs that can be connected at a time to an ADC that is integrated with successive approximation is
Option A:	4
Option B:	2
Option C:	8
Option D:	16
Q5.	Total interrupt vector table is divided into how many groups?
Option A:	2
Option B:	3
Option C:	4
Option D:	5

University of Mumbai
Examination 2020 under cluster 9 (FAMT)

Q6.	If a device after being serviced becomes the lowest priority, and consecutive next interrupt becomes highest priority. Then 8259 is operating in which of the following priority mode?
Option A:	Fully Nested Mode
Option B:	Special Fully Nested Mode
Option C:	Automatic Rotation Priority Mode
Option D:	Special Masked Mode
Q7.	The Temp real format data representation consists of ____ bits
Option A:	16
Option B:	32
Option C:	64
Option D:	80
Q8.	Which input of CPU is activated by 8257, in response to peripheral DMA request
Option A:	HOLD
Option B:	SET
Option C:	CLEAR
Option D:	CLK
Q9.	In most of the cases, the method used for decoding that may be used to minimise the required hardware is
Option A:	non-linear decoding
Option B:	absolute decoding
Option C:	linear decoding
Option D:	NO OPERATION
Q10.	Base Pointer (BP) contains offset address of _____segment
Option A:	Data Segment
Option B:	Code Segment
Option C:	Stack Segment
Option D:	Extra Segment
Q11.	In the signal integrate phase, the differential input voltage between IN LO(input low) and IN HI(input high) pins is integrated by the internal integrator for a fixed period of
Option A:	256 clock cycles
Option B:	1024 clock cycles
Option C:	2048 clock cycles
Option D:	4096 clock cycles
Q12.	BHE (active low) of 8086 microprocessor signal is used to interface the
Option A:	Even Bank Memory
Option B:	Odd Bank Memory
Option C:	I/O

University of Mumbai
Examination 2020 under cluster 9 (FAMT)

Option D:	DMA
Q13.	Initially if CH-0 gains highest priority while CH-3 gains lowest priority. The channel which has just been serviced will get the lowest priority after DMA cycle & other channels move upto the next higher priority levels. Then 8257 is operating in which of the following mode?
Option A:	Rotating Priority Mode
Option B:	Fixed Priority Mode
Option C:	Extended Write Mode
Option D:	Autoload Mode
Q14.	How many pins does the 8255 PPI IC contains?
Option A:	24
Option B:	28
Option C:	40
Option D:	32
Q15.	What will be the contents of register AL after the following has been executed MOV BL,32 MOV AL,88 ADD AL,BL DAA
Option A:	20 and carry flag is set
Option B:	20 and carry flag is reset
Option C:	BA and carry flag is set
Option D:	BA and carry flag is reset
Q16.	In 8086 microprocessor the following has the highest priority among all type of interrupts
Option A:	NMI
Option B:	Div 0
Option C:	TYPE 255
Option D:	OVERFLOW
Q17.	The 80386 DX is.....bit microprocessor.
Option A:	16
Option B:	8
Option C:	24
Option D:	32
Q18.	In 8259, In automatic rotation , the device , after being serviced , receives the _____ priority
Option A:	Lowest
Option B:	Highest
Option C:	Intermediate

University of Mumbai
Examination 2020 under cluster 9 (FAMT)

Option D:	Cannot predict
Q19.	In 8259, the register that stores all the interrupt requests in it in order to serve them one by one on a priority basis is
Option A:	Interrupt Request Register
Option B:	In-Service Register
Option C:	Priority resolver
Option D:	Interrupt Mask Register
Q20.	In 8253, the counter starts counting only if
Option A:	GATE signal is low
Option B:	GATE signal is high
Option C:	CLK signal is low
Option D:	CLK signal is high
Q21.	In 8253, in control word register, if SC1=0 and SC0=1, then the counter selected is
Option A:	Counter 0
Option B:	Counter 1
Option C:	Counter 2
Option D:	Counter 3
Q22.	In BSR mode, only port C can be used to
Option A:	Set individual ports
Option B:	Set individual ports
Option C:	Set and reset individual ports
Option D:	Programmable I/O ports
Q23.	How many bits of data can be transferred between the 8255 PPI and the interfaced device at a time? or What is the size of internal bus of the 8255 PPI?
Option A:	16 bit
Option B:	8 bit
Option C:	32 bit
Option D:	10 bit
Q24.	The number of counters that are present in the programmable timer device 8254 is
Option A:	1

University of Mumbai
Examination 2020 under cluster 9 (FAMT)

Option B:	2
Option C:	3
Option D:	4
Q25.	In 8257, to indicate the I/O device that its request for the DMA transfer has been honoured by the CPU, the DMA controller pulls
Option A:	HLDA Signal
Option B:	HRQ Signal
Option C:	DACK (Active Low)
Option D:	DACK(Active High)