These are sample MCQs to indicate pattern, may or may not appeared in examination

UNIVERSITY OF MUMBAI

Examination 2020 under cluster 9 (FAMT)

Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name:Microprocessor

Time: 1hour Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The CS register stores instruction in ___ segment
Option A:	Code
Option B:	Stack
Option C:	Data
Option D:	Extra
Q2.	___ is used to write in the memory.
Option A:	RD
Option B:	WR
Option C:	RD/WR
Option D:	CLK
Q3.	If MN/MX is low then 8086 operates in ____ mode.
Option A:	Minimum
Option B:	Maximum
Option C:	Both
Option D:	Medium
Q4.	___ signal is generated by combining RD and WR signals with IO/M .
Option A:	Control
Option B:	Memory
Option C:	Register
Option D:	System
Q5.	An ____ is used to fetch one address.
Option A:	Decoder
Option B:	External decoder
Option C:	Internal encoder
Option D:	Register
Q6.	Pentium has _____ number of execution units
Option A:	1

Option B:	2
Option C:	4
Option D:	3
Q7.	Pentium has ___ & ____ pipelines
Option A:	U&V
Option B:	X&Y
Option C:	A&B
Option D:	C&D
Q8.	Data cache in Pentium is ____
Option A:	16KB
Option B:	8KB
Option C:	32KB
Option D:	64KB
Q9.	What should be OCW1 code(D7...D0) for PIC, if interrupt inputs IR0 to IR2 and IR5
Option A:	11011000
Option B:	11001100
Option C:	11011100
Option D:	11110110
Q10.	In PIC, this interrupt has highest priority.
Option A:	IR0
Option B:	IR1
Option C:	IR7
Option D:	IR2
Q11.	An initialization control word, which is not used in single mode operation of PIC is
Option A:	ICW1
Option B:	ICW2
Option C:	ICW3
Option D:	ICW4
Q12.	Select true statement from the following options.
Option A:	ROM is nonvolatile and temporary memory
Option B:	RAM is volatile and permanent memory
Option C:	RAM is volatile and temporary memory.
Option D:	ROM is volatile and permanent memory
Q13.	In BSR mode, only PORT C can be used to
Option A:	set individual port
Option B:	reset individual port

Option C:	set and reset individual port
Option D:	program IO ports
Q14.	If a number of instructions are repeating through the main program, then to reduce
Option A:	procedure
Option B:	subroutine
Option C:	macro
Option D:	routine
Q15.	Which addressing mode execute its instructions within CPU without the necessity of
Option A:	Implied mode
Option B:	Immediate mode
Option C:	Direct Mode
Option D:	Register Mode
Q16.	The operands source and destination in an instruction cannot be
Option A:	register, register
Option B:	memory location, memory location
Option C:	memory location,register
Option D:	immediate data, register
Q17.	BIOS ia an acronym for
Option A:	Basic Input/Output System
Option B:	Base Input/Output System
Option C:	Base Interrupt Output system
Option D:	Basic Interrupt Output system
Q18.	The operands of an instruction cannot be
Option A:	register
Option B:	memory operands and immediate operands
Option C:	immediate operands
Option D:	memory operands
Q19.	If the interrupt is generated by the execution of an interrupt instruction then it is
Option A:	internal interrupt
Option B:	external interrupt
Option C:	interrupt-in-interrupt
Option D:	only interupt
Q20.	The type of the interrupt may be passed to the interrupt structure of CPU from
Option A:	interrupt service routine
Option B:	stack
Option C:	interrupt controller
Option D:	overflow interrupt

Q21.	Whenever a number of devices interrupt a CPU at a time, and if the processor is
Option A:	interrupt handling ability
Option B:	interrupt processing ability
Option C:	multiple interrupt processing ability
Option D:	multiple interrupt executing ability
Q22.	For the INTR signal, to be responded to in the next instruction cycle, it must go
Option A:	high
Option B:	low
Option C:	high or low
Option D:	high or low
Q23.	80386DX is available in a grid array package of
Option A:	16 pins
Option B:	128 pins
Option C:	132 pins
Option D:	142 pins
Q24.	Which unit in 80386 DX architecture plays a crucial role in the conversion of linear
Option A:	Execution
Option B:	Protection
Option C:	Segmentation
Option D:	Paging
Q25.	If the paging unit is enabled, then it converts a linear address into
Option A:	effective address
Option B:	physical address
Option C:	segment base address
Option D:	data address