These are sample MCQs to indicate pattern, may or may not appeared in examination

University of Mumbai
Online Examination 2020

Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2012

Examination: Third Year Semester VI

Course Code: ETC 606 and Course Name: VLSI DESIGN

Time: 1hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks.

Q1.	Considering the area requirement, 2 i/p NAND and 2 i/p NOR, which one is preferred
Option A:	NAND requires less area
Option B:	NOR requires less area
Option C:	Both requires same area
Option D:	NAND requires twice that of NOR area
Q2.	Number of access transistors present in SRAM cell
Option A:	One
Option B:	Two
Option C:	Three
Option D:	Four
Q3.	Increasing Vsb _____ the threshold voltage.
Option A:	does not effect b) decreases c) increases d) exponentially increases
Option B:	decreases
Option C:	increases
Option D:	exponentially increases
Q4.	Capacitor charge stored as information in DRAM will leak off or dissipated due to

Option A:	Leakage effect
Option B:	Charge effect
Option C:	Dynamic effect
Option D:	Static effect
Q5.	2 input CMOS AND gate will require
Option A:	2 n MOS and 2 p MOS transistors
Option B:	2 n MOS and 3 p MOS transistors
Option C:	3 n MOS and 2 p MOS transistors
Option D:	3 n MOS and 3 p MOS transistors
Q6.	α is used for scaling
Option A:	linear dimensions
Option B:	Vdd
Option C:	oxide thickness
Option D:	non linear dimensions
Q7.	Surface mobility depends on _____
Option A:	effective drain voltage
Option B:	effective gate voltage
Option C:	channel length
Option D:	effective source voltage
Q8.	Positive photo resists are used more than negative photo resists because _____
Option A:	Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists
Option B:	Positive photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the negative photo resists
Option C:	Negative photo resists are less sensitive to light
Option D:	Positive photo resists are less sensitive to light

Q9.	If the n-MOS and p-MOS of the CMOS inverters are interchanged the output is measured at:
Option A:	Source of both transistor
Option B:	Drains of both transistor
Option C:	Drain of n-MOS and source of p-MOS
Option D:	Source of n-MOS and drain of p-MOS
Q10.	The overall delay of n MOS inverter pair is?
Option A:	4τ
Option B:	τ
Option C:	5τ
Option D:	2τ
Q11.	Rise time and fall time is _____ to Vdd.
Option A:	directly proportional
Option B:	inversely proportional
Option C:	exponentially equal
Option D:	not related
Q12.	According to body effect, substrate is biased with respect to _____
Option A:	source
Option B:	drain
Option C:	gate
Option D:	Vss
Q13.	The asymmetry of resistance value can be eliminated by _____
Option A:	decreasing the width
Option B:	Increasing the width
Option C:	increasing the length
Option D:	increasing the width
Q14.	Which color is used for n-diffusion?
Option A:	red
Option B:	blue
Option C:	green
Option D:	yellow
Q15.	Implant is represented using _____
Option A:	black, dark line
Option B:	black, dotted line
Option C:	yellow, dark line

Option D:	yellow, dotted line
Q16.	As die size shrinks, the complexity of making the photo masks _____
Option A:	increases
Option B:	decreases
Option C:	remains the same
Option D:	cannot be determined
Q17.	What is the design flow of VLSI system?
Option A:	architecture design
Option B:	market requirement
Option C:	logic design
Option D:	HDL coding
Q18.	Which provides higher integration density?
Option A:	switch transistor logic
Option B:	transistor buffer logic
Option C:	transistor transistor logic
Option D:	circuit level logic
Q19.	Positive photo resists are used more than negative photo resists because _____
Option A:	Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists
Option B:	Positive photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the negative photo resists
Option C:	Negative photo resists are less sensitive to light
Option D:	Positive photo resists are less sensitive to light
Q20.	The dopants are introduced in the active areas of silicon by using which process?
Option A:	Diffusion process
Option B:	Ion Implantation process
Option C:	Chemical Vapour Deposition
Option D:	Either Diffusion or Ion Implantation Process
Q21.	Clock signal Φ2 is to
Option A:	write data
Option B:	read data
Option C:	refresh data
Option D:	store data
Q22.	Which occupies lesser area?
Option A:	N MOS
Option B:	P MOS

Option C:	CMOS
Option D:	Bi CMOS
Q23.	Current flows only when
Option A:	RD is low
Option B:	RD is high
Option C:	RD raises exponentially high
Option D:	RD comes exponentially down
Q24.	Data is read
Option A:	before Φ1
Option B:	after Φ1
Option C:	before Φ2
Option D:	after Φ2
Q25.	Which clock is preferred in storage devices?
Option A:	single phase overlapping clock signal
Option B:	single phase non overlapping clock signal
Option C:	two phase overlapping clock signal
Option D:	two phase non overlapping clock signal