These are sample MCQs to indicate pattern, may or may not appear in examination

University of Mumbai
Online Examination 2020

Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester VI

Course Code: ECCDLO6021 and Course Name: Digital VLSI Design

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	The required threshold voltage(VGS) of an N Channel enhancement mode MOSFET to turn it ON is need to be ……
Option A:	Positive
Option B:	Negative
Option C:	Can be both negative as well as positive
Option D:	Indeterministic
Q2.	Mobility of electrons is …….
Option A:	Half of mobility of holes
Option B:	Same as mobility of holes
Option C:	About Twice of mobility of holes
Option D:	Unpredictable till date
Q3.	Advantage of static CMOS circuit is
Option A:	Full swing output
Option B:	Low swing
Option C:	Cheap
Option D:	Easy to built
Q4.	Pseudo NMOS logic is
Option A:	Ratioed logic
Option B:	Non Ratioed logic
Option C:	Tristate logic
Option D:	Unused logic
Q5.	Which of following are CMOS Layout scalable design rules?
Option A:	Thickness rules
Option B:	Micron rules
Option C:	Layer rules
Option D:	Lambda rules

Q6.	1T DRAM cell contain
Option A:	1 MOSFET and a storage capacitor
Option B:	3 MOSFETs
Option C:	One capacitor only
Option D:	6 MOSFETS
Q7.	Memory element in SRAM is
Option A:	Capacitor
Option B:	Flip Flop
Option C:	Resistor
Option D:	Inductor
Q8.	Which of following is Random Access Memory
Option A:	EPROM
Option B:	EEPROM
Option C:	PROM
Option D:	SRAM
Q9.	What is common with RAM array and ROM array
Option A:	Individual memory cells can be accessed for data read and/or data write operations in random order, independent of their physical locations in the memory array.
Option B:	Individual memory cells can be accessed for data read and/or data write operations in sequential order, independent of their physical locations in the memory array.
Option C:	Individual memory cells can be accessed for data read operations only in sequential order, independent of their physical locations in the memory array.
Option D:	Individual memory cells can be accessed for data write operations only in sequential order, independent of their physical locations in the memory array.
Q10.	Which adder is faster? Ripple carry adder or Carry look ahead adder?
Option A:	Both are slow
Option B:	Both are fast
Option C:	RCA is faster than CLA
Option D:	RCA is slower than CLA for large addition
Q11.	In full Adder with three inputs A,B, Cin. Where Cin is carry out value of previous stage. Generate term Gk is calculated by
Option A:	A OR B
Option B:	A AND B
Option C:	A XOR B
Option D:	A XNOR B
Q12.	Advantage of Carry Select Adder is
Option A:	Speed Improvement

Option B:	Small size
Option C:	Less hardware
Option D:	Easy to built
Q13.	Barrel Shifter is
Option A:	UML Diagram
Option B:	Sequential circuit
Option C:	Data flow graph
Option D:	Combinational circuit
Q14.	Hold time is defined as the time required for the data to _____ after the triggering edge of clock.
Option A:	Increase
Option B:	Decrease
Option C:	Remain stable
Option D:	Exponential
Q15.	In fusible link technologies, the undesired fuses are removed by the pulse application of _____voltage & current to device input.
Option A:	High
Option B:	Moderate
Option C:	Low
Option D:	Negative
Q16.	Increase in the physical distance of H-tree _____the skew rate.
Option A:	Decreases
Option B:	Increases
Option C:	Stabilizes
Option D:	Distorted
Q17.	In VHDL, which class of scalar data type represents the values necessary for a specific operation?
Option A:	Integer types
Option B:	Enumerated types
Option C:	Physical types
Option D:	Real types
Q18.	In testability, which terminology is used to represent or indicate the formal evidences of correctness?
Option A:	Simulation
Option B:	Validation
Option C:	Verification
Option D:	Integration
Q19.	In floorplanning, placement and routing are _____ tools.
Option A:	Back end

Option B:	Front end
Option C:	Right End
Option D:	Bottom End
Q20.	Which type of CPLD packaging comprises pins on all four sides that wrap around the edges of chip?
Option A:	Plastic-Leaded Chip Carrier (PLCC)
Option B:	Quad Flat Pack (QFP)
Option C:	Ceramic Pin Grid Array (PGA)
Option D:	Ball Grid Array (BGA)
Q21.	In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance?
Option A:	Static dissipation
Option B:	Positive Dissipation
Option C:	Dynamic dissipation
Option D:	Negative Dissipation
Q22.	The devices which are based on fusible link or antifuse are _____time/s programmable.
Option A:	one
Option B:	two
Option C:	four
Option D:	infinite
Q23.	Which among the following is not suitable for in-system programming?
Option A:	PROM
Option B:	EEPROM
Option C:	Flash
Option D:	RAM
Q24.	Which type of digital systems exhibit the necessity for the existence of at least one feedback path from output to input?
Option A:	Combinational System
Option B:	Data flow
Option C:	Sequential system
Option D:	Arithmetic
Q25.	The power consumption of static CMOS gates varies with the _____ of power supply voltage.
Option A:	cube
Option B:	square
Option C:	fourth power
Option D:	1/8 th power