Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: ECC501 and Course Name: MPI

Time: 1 hour Max. Marks: 20

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	If there are N address lines, then it can address how many memory locations?
Option A:	2^N
Option B:	2^(N-1)
Option C:	(2-1)^N
Option D:	N^2
Q2.	A processor has 4 GB memory, how many address lines are required to access this memory?
Option A:	2^16
Option B:	2^32
Option C:	2^8
Option D:	2^16
Q3.	Identify which from the following is not High Level Language
Option A:	8086 Assembly Language
Option B:	C++
Option C:	FORTRAN
Option D:	BASIC
Q4.	What is the main function of Priority Resolver of 8259?
Option A:	Store the masking pattern of interrupts
Option B:	Determine highest Priority interrupt
Option C:	Store level of Interrupt Request currently being serviced
Option D:	Control the other blocks
Q5.	When MSB of the result is 1 which flag is set
Option A:	Zero Flag(ZF)

Option B:	Sign Flag(SF)
Option C:	Parity Flag(PF)
Option D:	Overflow Flag(OF)
Q6.	Which pin of 8257 Programmable DMA controller clears mode set register and status register, and forces 8257 into slave mode
Option A:	CLEAR
Option B:	READY
Option C:	HLDA
Option D:	RESET
Q7.	8086 Execution unit has four general purpose…….registers
Option A:	8 bit
Option B:	64 bit
Option C:	16 bit
Option D:	32 bit
	16 bit
Q8.	Which from the following works as a default counter register for string & loop operations
Option A:	Ax
Option B:	Bx
Option C:	Cx
Option D:	Dx
Q9.	Identify the physical address for MOV Ax,[Bx+SI+06H] Assume, DS=2100H, Bx=0158H, SI=3050H
Option A:	241AEH
Option B:	241AFH
Option C:	241A8H
Option D:	2418AH
Q10.	S3 & S4 gives the status of the memory segment currently accessed. What is the status of S3 & S4 to access Stack Segment
Option A:	S3=0, S4=0
Option B:	S3=1, S4=0
Option C:	S3=0, S4=1
Option D:	S3=1, S4=1
Q11.	In 8086, one bank contains all even addresses called……& …….. containing all odd addresses.
Option A:	Lower bank, Upper bank
Option B:	Upper bank, Lower bank
Option C:	Odd bank, Even bank
Option D:	Even bank, Lower bank

Q12.	If in case of 8255 following instructions are given: MOV AL, 95H; OUT CWR, AL; Then select the status of 8255 ports.
Option A:	Initialize port A as input, port B as output, port C upper as output & port C lower as input
Option B:	Initialize port A as output, port B as input, port C upper as output & port C lower as input
Option C:	Initialize port A as input, port B as output, port C upper as input & port C lower as output
Option D:	Initialize port A as input, port B as output, port C upper as output & port C lower as output
Q13.	Which of the following signalis not generated by 8288 bus controller
Option A:	ALE
Option B:	I/O Read
Option C:	BHE’
Option D:	DEN
Q14.	Identify the instruction which is having Register Indirect addressing mode
Option A:	MOV [SI], Bx
Option B:	MOV Bx, Cx
Option C:	SUB Cl, [Bx+SI]
Option D:	ADD Ax, Bx
Q15.	Which pin is enabled to begin A to D conversion?
Option A:	ALE
Option B:	START
Option C:	EOC
Option D:	OE
Q16.	Main function of……is decoding & execution of the instruction
Option A:	Execution Unit
Option B:	Bus Interface Unit
Option C:	Instruction Byte Queue
Option D:	Memory unit
Q17.	If Total RAM=32KB, chip available=8KB, then how many sets are required?
Option A:	1
Option B:	2
Option C:	4
Option D:	8
Q18.	The pin that disables all the DMA channels by clearing the mode registers is
Option A:	MARK
Option B:	CLEAR

Option C:	RESET
Option D:	READY
Q19.	EPROM required is 32KB, available chil size=8KB, then how many chips required?
Option A:	2
Option B:	3
Option C:	4
Option D:	8
Q.20	The register that stores the bits required to mask the interrupt inputs is
Option A:	In-service register
Option B:	Priority resolver
Option C:	Interrupt Mask register
Option D:	None
Q.21	For selection of counter 0 , what should be the status of A0-A1
Option A:	00
Option B:	01
Option C:	10
Option D:	11
Q.22	What is mode 3 of 8254?
Option A:	Pulse generator
Option B:	Square wave generator
Option C:	Software trigger strobe
Option D:	Interrupt on terminal count
Q.23	In BSR mode, only port C can be used to
Option A:	set individual ports
Option B:	reset individual ports
Option C:	set and reset individual ports
Option D:	programmable I/O ports
Q.24	In 8086, which locations are reserved for IVT?
Option A:	0000H to 03FFH
Option B:	0000H to 03FFE
Option C:	00000H to 003FFH
Option D:	00000H to FFFFFH
Q.25	In which type of interrupt gets generated if the result of DIV or IDIV operation is too large to fit destination register?
Option A:	Type0
Option B:	Type1
Option C:	Type2
Option D:	Type3