University of Mumbai
Examination 2020 under cluster 9 (FAMT)

Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2016

Examination: Second Year Semester III

Course Code: ECC303 and Course Name: DIGITAL SYSTEM DESIGN

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	On subtracting (01010)2 from (11110)2 using 1's complement, we get _____
Option A:	01001
Option B:	11010
Option C:	10101
Option D:	10100
Q2.	The expression for Absorption law is given by _____
Option A:	A + AB = A
Option B:	A + AB = B
Option C:	AB + AA' = A
Option D:	A + B = B + A
Q3.	The number of full and half adders are required to add 16-bit number is _____
Option A:	8 half adders, 8 full adders
Option B:	1 half adders, 15 full adders
Option C:	16 half adders, 0 full adders
Option D:	4 half adders, 12 full adders
Q4.	The following switching functions are to be implemented using a decoder: f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7) The minimum configuration of decoder will be _____
Option A:	2 to 4 line
Option B:	3 to 8 line
Option C:	4 to 16 line
Option D:	5 to 32line
Q5.	Which of the following logic families has the highest maximum clock frequency?
Option A:	S-TTL
Option B:	AS-TTL
Option C:	HS-TTL

Option D:	HCMOS
Q6.	In a sequential circuit, the output at any time depends only on the input values at that time.
Option A:	Past output values
Option B:	Intermediate values
Option C:	Both past output and present input
Option D:	Present input values
Q7.	On addition of -33 and -40 using 2's complement, we get _____
Option A:	1001110
Option B:	-110101
Option C:	0110001
Option D:	-1001001
Q8.	DeMorgan's theorem states that _____
Option A:	(AB)' = A' + B'
Option B:	(A + B)' = A' * B
Option C:	A' + B' = A'B'
Option D:	(AB)' = A' + B
Q9.	The code where all successive numbers differ from their preceding number by single bit is _____
Option A:	Alphanumeric Code
Option B:	BCD
Option C:	Excess 3
Option D:	Gray
Q10.	How many NAND circuits are contained in a 7400 NAND IC?
Option A:	2
Option B:	4
Option C:	8
Option D:	16
Q11.	According to the IC fabrication process logic families can be divided into two broad categories as:
Option A:	RTL and TTL
Option B:	HTL and MOS
Option C:	ECL and DTL
Option D:	Bipolar and MOS
Q12.	Which statement below best describes a Karnaugh map?
Option A:	It is simply a rearranged truth table
Option B:	The Karnaugh map eliminates the need for using NAND and NOR gates
Option C:	Variable complements can be eliminated by using Karnaugh maps
Option D:	A Karnaugh map can be used to replace Boolean rules

Q13.	Binary coded decimal is a combination of _____
Option A:	Two binary digits
Option B:	Three binary digits
Option C:	Four binary digits
Option D:	Five binary digits
Q14.	A modulus-10 counter must have _____
Option A:	10 flip-flops
Option B:	4 flip-flops
Option C:	8 flip-flops
Option D:	2 flip-flops
Q15.	What distinguishes the look-ahead-carry adder?
Option A:	It is slower than the ripple-carry adder
Option B:	It is easier to implement logically than a full adder
Option C:	It is faster than a ripple-carry adder
Option D:	It requires advance knowledge of the final answer
Q16.	In a multiplexer, the selection of a particular input line is controlled by _____
Option A:	Data controller
Option B:	Selected lines
Option C:	Logic gates
Option D:	Both data controller and selected lines
Q17.	When a high is applied to the Set line of an SR latch, then _____
Option A:	Q output goes high
Option B:	Q' output goes high
Option C:	Q output goes low
Option D:	Both Q and Q' go high
Q18.	Which of the following is the basic building block of a design?
Option A:	Architecture
Option B:	Entity
Option C:	Process
Option D:	Package
Q19.	CMOS refers to _____
Option A:	Continuous Metal Oxide Semiconductor
Option B:	Complementary Metal Oxide Semiconductor
Option C:	Centred Metal Oxide Semiconductor
Option D:	Concrete Metal Oxide Semiconductor
Q20.	A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW.

	The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____
Option A:	1110
Option B:	0111
Option C:	1000
Option D:	1001
Q21.	There are _____ cells in a 4-variable K-map.
Option A:	4
Option B:	8
Option C:	16
Option D:	32
Q22.	In 1-to-4 demultiplexer, how many select lines are required?
Option A:	2
Option B:	3
Option C:	4
Option D:	5
Q23.	Propagation delay is defined as _____
Option A:	the time taken for the output of a gate to change after the inputs have changed
Option B:	the time taken for the input of a gate to change after the outputs have changed
Option C:	the time taken for the input of a gate to change after the intermediates have changed
Option D:	the time taken for the output of a gate to change after the intermediates have changed
Q24.	How many inputs will a decimal-to-BCD encoder have?
Option A:	4
Option B:	8
Option C:	10
Option D:	16
Q25.	In VHDL, Bus is a type of _____
Option A:	Signal
Option B:	Constant
Option C:	Variable
Option D:	Driver