Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2012

Examination: Second Year Semester IV

Course Code: ETC402, Course Name: AE-II

Time: 1 hour Max. Marks: 25

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Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	What term means that the midrange voltage gain is assigned a value of 1 (or 0 dB)?
Option A:	critical
Option B:	Miller
Option C:	normalized
Option D:	corner
Q2.	In a multistage amplifier, the overall frequency response is determined by the
Option A:	frequency response of each stage depending on the relationships of the critical frequencies.
Option B:	frequency response of the first amplifier.
Option C:	frequency response of the last amplifier.
Option D:	lower critical frequency of the first amplifier and the upper critical frequency of the final amplifier
Q3.	An amplifier has an input signal voltage of 0.054 mV. The output voltage is 12.5 V. The voltage gain in dB is
Option A:	6 dB.
Option B:	107.3 dB.
Option C:	231 dB.
Option D:	116 dB.
Q4.	A roll-off of 20 dB per decade is equivalent to a roll-off of _____ per octave.
Option A:	3 dB
Option B:	13 dB
Option C:	12 dB
Option D:	6 dB
Q5.	Internal transistor junction capacitances affect the high-frequency response of amplifiers by
Option A:	reducing the amplifier’s gain.
Option B:	introducing phase shift as the signal frequency increases.

Option C:	having no effect.
Option D:	reducing the amplifier's gain and introducing phase shift as the signal frequency increases.
Q6.	Each RC circuit causes the gain to drop at a rate of _____ dB/decade.
Option A:	20
Option B:	10
Option C:	6
Option D:	2
Q7.	In ideal Differential Amplifier, if same signal is given to both inputs, then output will be
Option A:	Same as input
Option B:	Double the input
Option C:	Not equal to zero
Option D:	Zero
Q8.	An emitter bias Dual Input Balanced Output differential amplifier has VCC=20v, β=100, VBE=0.7v, RE=1.3kΩ. Find IE
Option A:	7.42mA
Option B:	9.8mA
Option C:	10mA
Option D:	8.6mA
Q9.	Obtain the collector voltage, for collector resistor (RC) =5.6kΩ, IE=1.664mA and VCC=10v for single input unbalanced output differential amplifier
Option A:	0.987v
Option B:	0.682v
Option C:	0.555v
Option D:	0.89v
Q10.	Find Common Mode Rejection Ration, given gm =16MΩ-1, RE=25kΩ
Option A:	58 db
Option B:	40 db
Option C:	63 db
Option D:	89 db
Q11.	If the value of Common Mode Rejection Ratio and Common Mode Gain are 40db and -0.12 respectively, then determine the value of differential mode gain
Option A:	0.036
Option B:	-1.2
Option C:	4.8
Option D:	12
Q12.	Ideal op-amp has infinite voltage gain because

Option A:	To control the output voltage
Option B:	To obtain finite output voltage
Option C:	To receive zero noise output voltage
Option D:	To obtain infinite output voltage
Q13.	Find the output voltage of an ideal op-amp. If V1 and V2 are the two input voltages
Option A:	VO= V1-V2
Option B:	VO= A×(V1-V2)
Option C:	VO= A×(V1+V2)
Option D:	VO= V1×V2
Q14.	Find the output of inverting amplifier?
Option A:	Vo = AVin
Option B:	Vo = -AVin
Option C:	Vo = -A(Vin1– Vin2)
Option D:	Vo = -A(Vin1+ Vin2)
Q15.	Which is not the ideal characteristic of an op-amp?
Option A:	Input Resistance => 0
Option B:	Output impedance => 0
Option C:	Bandwidth => ∞
Option D:	Open loop voltage gain => ∞
Q16.	In practical application of current mirror, early voltage is assumed to be
Option A:	Infinite
Option B:	Zero
Option C:	Unity
Option D:	Non zero
Q17.	A widlar current source is used
Option A:	to get low value of current
Option B:	to get high value of CMRR
Option C:	to get low voltage of gain
Option D:	to get high value of Output
Q18.	Which current source exhibits a very high output resistance?
Option A:	Simple current mirror
Option B:	Wilson current mirror
Option C:	Widlar current mirror
Option D:	current mirror using swamping resistor
Q19.	Introducing FET differential amplifier pair at the input stage of differential amplifier produces
Option A:	High output resistance

Option B:	High input resistance
Option C:	Low input impedance
Option D:	Low output resistance
Q20.	Transistor in power amplifier is _____
Option A:	An active device
Option B:	A passive device
Option C:	A op-amp
Option D:	A voltage generating device
Q21.	Which of the following amplifier class have highest linearity and lowest distortion?
Option A:	Class A
Option B:	Class B
Option C:	Class C
Option D:	Class B push-pull
Q22.	Which of the following amplifier cannot be used for audio frequency amplification?
Option A:	Class A
Option B:	Class C
Option C:	Class AB
Option D:	Class B push-pull
Q23.	Amplitude distortion is due to _____
Option A:	Shift in Q-point
Option B:	Change in input
Option C:	Linear amplification
Option D:	Small input signal
Q24.	Frequency distortion occurs when _____ is varied with frequency.
Option A:	Amplitude
Option B:	Amplification
Option C:	Distortion
Option D:	Output
Q25.	In a class B amplifier, it is found that DC power is 25W, find the ac power.
Option A:	10 W
Option B:	62.5 W
Option C:	25 W
Option D:	50 W