These are sample MCQs to indicate pattern, may or may not appear in examination

University of Mumbai

Online Examination 2020

Program: TE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name: Microprocessor Time: 1hour Max. Marks: 50

Note to the students:- All the Questions are compulsory and carry equal marks .

Q1.	_____ converts the programs written in assembly language into machine instructions.
Option A:	Machine compiler
Option B:	Interpreter
Option C:	Assembler
Option D:	Converter

Q2.	If there is a carry from lowest nibble during addition, _____ flag sets.
Option A:	Carry
Option B:	Auxiliary carry
Option C:	Over flow
Option D:	Sign

Q3.	To obtain 16bit data bus width, the two 4k*8 chips of RAM and ROM are arranged in
Option A:	Serial
Option B:	Parallel
Option C:	serial as well as parallel
Option D:	parallel followed by serial

Q4.	To address a memory location out of N locations, number of address lines required is
Option A:	log N (base 2)
Option B:	log N (base 10)
Option C:	log N (base e)
Option D:	log 2N (base e)

Q5.	In 8086 microprocessor the following has the highest priority among all type interrupts.
Option A:	NMI
Option B:	DIV 0
Option C:	TYPE 255
Option D:	OVER FLOW

Q6.	In PPI, handshaking signals are generated by
Option A:	PORT A
Option B:	PORT B
Option C:	PORT C
Option D:	GROUP A

Q7.	Instruction Pointer (IP) contains offset address of _____ segment.

Option A:	Data segment
Option B:	Code segment
Option C:	Stack segment
Option D:	Extra segment

Q8.	8086 is interfaced to two 8259s (Programmable interrupt controllers). If 8259s are in master slave configuration the number of interrupts available to the 8086 microprocessor is _____.
Option A:	8
Option B:	16
Option C:	15
Option D:	64

Q9.	Pentium has following pipelines.
Option A:	AB
Option B:	XY
Option C:	PQ
Option D:	UV

Q10.	If the size of the segment is 64 kb, what will be the starting and ending off set addresses of it
Option A:	0000H to 7FFFH
Option B:	0000H to FFFFH
Option C:	8000H to FFFFH
Option D:	00000H to FFFFFH

Q11.	Which of the following instruction is not valid?
Option A:	MOV AX, BX
Option B:	MOV DS, 5000H
Option C:	MOV AX, 5000H
Option D:	PUSH AX

Q12.	PIC works in Special Fully Nested Mode , if this data bit is set to 1 in ICW4.
Option A:	D1
Option B:	D2
Option C:	D3
Option D:	D4

Q13.	BIU Prefetch the instruction from memory and store them in _____
Option A:	Instruction queue
Option B:	Instruction Pointer
Option C:	Stack Pointer
Option D:	Memory

Q14.	How much virtual memory can be accessed by 80386 microprocessor?
Option A:	1MB
Option B:	4MB
Option C:	4GB
Option D:	64TB

Q15.	Which of the following is not a data copy/transfer instruction?
Option A:	MOV
Option B:	PUSH
Option C:	DAS
Option D:	POP

Q16.	The _____ translates a byte from one code to another code
Option A:	XLAT
Option B:	XCHNG
Option C:	POP
Option D:	PUSH

Q17.	If the paging unit is enabled, then it converts a linear address into
Option A:	effective address
Option B:	physical address
Option C:	segment base address
Option D:	Offset address

Q18.	Which is a correct statement from the following?
Option A:	u pipe executes simple instructions only
Option B:	v pipe executes simple instructions only
Option C:	v pipe executes simple and complex instructions
Option D:	Floating point instructions can be paired

Q19.	In memory interfacing, following component is used for memory chip selection.
Option A:	Transceiver
Option B:	Bus Controller
Option C:	Timer
Option D:	Decoder

Q20.	What does it mean by bubble in pipeline?
Option A:	Flushing and reloading of pipeline
Option B:	Executing the instruction from pipeline
Option C:	Decoding instruction from pipeline
Option D:	No reloading of pipeline

Q21.	Direction flag is used with ____.
Option A:	String instructions
Option B:	Stack Instructions
Option C:	Arithmetic Instructions
Option D:	Branch Instructions

Q22.	An initialization control word, which is not used in single mode operation of PIC is
Option A:	ICW1
Option B:	ICW2
Option C:	ICW3

Option D:	ICW4

Q23.	MESI protocol requires Pentium to monitor all accesses to main memory in multiprocessor system. It is called
Option A:	Consistency
Option B:	Coherency
Option C:	Reliability
Option D:	Bus snooping

Q24.	_____ register is used as a default counter in case of string and loop instructions.
Option A:	AX
Option B:	BX
Option C:	CX
Option D:	DX

Q25.	What does indicate exclusive state of cache memory?
Option A:	The current line has been modified and available in single cache
Option B:	The current line has not been modified and available in single cache
Option C:	The current line has been modified and available in more than one cache
Option D:	The current line has not been modified and available in more than one cache