## These are sample MCQs to indicate pattern, may or may not appear in examination

## **University of Mumbai Online Examination 2020**

Program: SE Computer Engineering Curriculum Scheme: Revised 2016 Examination: Second Year Semester III

Course Code: CSC302 and Course Name: Digital Logic Design and Analysis Time: 1hour

Max. Marks: 50

Note to the students. All the Questions are somewhere and some social walls		
Note to the students:- All the Questions are compulsory and carry equal marks .		
Q1.	Which is a correct statement?	
Option A:	Digital signal has low noise immunity than analog signal.	
Option B:	Analog signal consumes more power during transmission than digital signal.	
Option C:	Digital system is more accurate compared to analog system.	
Option D:	Digital system is easily prone to errors.	
Q2.	this input is forbidden from SR flip flop.	
Option A:	00	
Option B:	01	
Option C:	10	
Option D:		
Q3.	Page around condition occurs in the flex	
	Race around condition occurs inflip flop.	
Option A:	SR	
Option B:	JK	
Option C:	D	
Option D:	T	
Q4.	What is 2's complement of 1000 1100?	
Option A:	0111 0011	
Option B:	0111 0001	
Option C:	0111 0100	
Option D:	0111 0101	
Q5.	If input lines are N and Selection lines are M of multiplexer, how to represent relationship between them?	
Option A:	N= log M (base 2)	
Option B:	M= log N (base 2)	
Option C:	N= log M (base 10)	
Option D:	M= log M (base 10)	
Q6.	What is a correct statement?	
Option A:	AND gate has same output as XNOR	
Option B:	OR gate has same output as XNOR	
Option C:	NAND gate has same output as bubbled OR	
Option D:	NAND gate has same output as bubbled XOR	

Q7.	In base (2's, 8's, 16's) complement subtraction, after adding base complement of
	subtrahend to minuend, if carry is generated, then

Option A:	carry is added to the sum, to get answer in original form.
Option B:	carry is ignored.
Option C:	result is negative so calculate its base complement
Option D:	result is positive and answer is not in its original form
Q8.	In (base-1) complement subtraction(1's,7's and 15's C subtraction), after adding (base-1)
	complement of subtrahend to minuend, if carry is generated, then
Option A:	carry is added to the sum, to get answer in original form.
Option B:	result is positive and answer is in its original form
Option C:	result is negative so calculate its (base-1) complement
Option D:	carry is ignored
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Q9.	In half adder, carry is generated by
Option A:	ORing two input operands
Option B:	XORing two input operands
Option C: Option D:	XNORing two input operands
Option D.	ANDing two input operands
Q10.	Which is correct statement regarding decoder?
Option A:	Number of input lines are more than number of output lines.
Option B:	Input lines are active low
Option C:	Output lines are active low
Option D:	Any number of output lines decoder can have , irrespective of number of input lines.
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Q11.	Full adder is implemented using half adder by using
Option A:	one half adder and one AND gate
Option B:	two half adders and one OR gate
Option C:	one half adder and one OR gate
Option D:	two half adders and one AND gate
Q12.	Binary code for (1110)gray code is
Option A:	1010
Option B:	1011
Option C:	1100
Option D:	0101
042	
Q13.	Gray code for binary code (1011) is
Option A:	1010
Option B:	0111
Option C:	1110
Option D:	0101
Q14.	What is result of (22) 4 + (22) 4 (add two numbers from been 4)2
Option A:	What is result of (23) 4 + (32) 4, (add two numbers from base 4)?
Option B:	(31)4
Option C:	(21)4
	(121)4
Option D:	(131)4

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Option D:	0011
Q23.	What is radix of numbering system which supports 0,1,2,3?
Option A:	3
Option B:	4
Option C:	5
Option D:	6
Q24.	What is the result of $(45)8 + (23)8$ ?
Option A:	(67)8
Option B:	(70)8
Option C:	(66)8
Option D:	(77)8
Q25.	What is (78)H + (B9)H?
Option A:	(131)H
Option B:	(31)H
Option C:	(13A)H
Option D:	(A31)H